Al-Al Bayt University
Prince Hussein bin Abdullah Faculty of Information Technology
Computer Science

Course Title : Digital Logic Design
Course Number :901220
Credit Hours :3
Pre requisite :
Placement :
Instructor: , w_qassas@aabu.edu.jo Sunday, Tuseday, Thursday 10:00-11:00, or by appointment,

Course Description :

This course provides a modern introduction to logic design and the basic building blocks used in digital systems, in particular digital computers. It starts with a discussion of combinational logic: logic gates, minimization techniques, arithmetic circuits, and modern logic devices such as field programmable logic gates. The second part of the course deals with sequential circuits: flip-flops, synthesis of sequential circuits, and case studies, including counters, registers, and random access memories. State machines will then be discussed and illustrated through case studies of more complex systems using programmable logic devices. Different representations including truth table, logic gate, timing diagram, switch representation, and state diagram will be discussed.

General objectives :

The Objective of this course is to familiarize the student with fundamental principles of digital design. It provides coverage of classical hardware design for both combinational and sequential logic circuits.
The course is supported by a digital logic design laboratory that uses the IDL-800 Digital Lab. device. This instrument is a circuit evaluator that enables users to design and connect standard Integrated Circuits.

Course outline :

Binary Systems
Digital Computers & Systems
Binary numbers
Number Base Conversion
Octal & Hexadecimal Numbers
1's & 2's Complements
Binary codes.
Boolean Algebra & Logical Gates
Basic Definitions
Boolean Algebra
Theorems of Boolean Algebra.
Boolean Functions
Digital Logic Gates.
IC Digital Logic Families
Simplification of Boolean Function
Karnaugh Map Method
3 variable , 4 variable, 5 variable Map.
Sum Of Product
Product of Sum
Dont care
Tabulation Method
Combinational Logic
Design Procedure
Adders

Subtractors
Code conversion
Analysis procedure.

chap1 to chap7

Fundamental building blocks of logic gates.
Bits, bytes, and words.
Numeric data representation and number bases.
Mathematical operations in different Numbering systems .
Signed and twos-complement representations.
Simplification of Boolean functions (algebraic method, Karnaugh maps, Quine McCluskey method) .
Logic expressions, minimization, sum of product forms.
Integrated combinatorial circuits.
Sequential circuits.
Flip-flops, registers, counters, memory units.

Evaluation methodology :

First Exam.....15
Second exam.....15
Lab experiments.....10
Mid practical/LAB.....10
Final practical/LAB.....10
Final exam.....40

References :

*Logic and Computer Design Fundamentals2nd edition, Prentice Hall,M. Mano
*Digital logic design3rd Ed., McHill,

Course Schedule :

Topic_____Hours

Syllabus review & Introduction----------1
Truth table and symbolic representation
Fundamental properties for Boolean algebra----------2
Implementing Circuits form Truth table , practice----------2
XOR gate, Demorgans Law
Logical expression simplification using Fundamental properties, Demorgan , Practice----------2
Karnaugh map (3 input, 4 input), SOP,POS, practice----------3
Tabulation method----------1
Numbering systems, Binary numbers, Hexadecimal,Coding, Error detection, real number implementation, IEE754----------4
Combinational circuits, Design procedure, Practice----------3
Combinational circuits, Analysis procedure, Practice----------2
MSI circuits, 4Bit full adder, Decoder, Multiplexer, comparator,
Building functions using MUX,or Decoder, building BCD to Ex-3 converter,----------4
First exam , Solution and discussion----------2
Design procedure
Examples using design procedure, Full adder, Full subtractor
BCD to Ex-3 code converter
4-bit ADDER/Subtractor using 4-bit Full adder,XOR gates,

Comparator----------4

Demultiplexter, Encoder,
Using Decoder for Implementing Logical functions
Using Multiplexer for implementing logical fuctions----------2
Sequential circuits characteristics,synchronous, Asynchronous circuits.
RS Latch(using NAND, using NOR gates),RS with Control, D Latch,
JK flipflop,T-Flip flop, Characteristic table & equations for Flip flops.----------5
Sequential circuits analysis procedure, Excitation table for the flip flops, Design procedure, Excitation table for sequential circuits,examples----------4
Using MSI 4 bit counter in building different counters
Registers and Memory unit, course review----------2